PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Eiichi TAKAHASHI et al.

Application No.: 10/520,429

Filed: July 13, 2005 Docket No.: 122358

For: DIGITAL CIRCUIT HAVING DELAY CIRCUIT FOR ADJUSTMENT OF CLOCK SIGNAL TIMING

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. The reference were cited in a counterpart foreign application.

☒ 3. A concise explanation of the relevance of the non-English language reference 4 appears in the Appendix attached hereto.

☒ 4. English language Abstracts of references 1-3 are attached hereto.

☒ 5. Computer-generated English language translations of the following Japanese references have been obtained from the website of the Japanese Patent Office ([http://www.jpo.go.jp]), and are attached, but have not been reviewed for accuracy. See References 1-3.

Respectfully submitted,

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JAO:PAC/nxy

Date: October 6, 2005

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Sheet 1 of 1

Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 122358	APPLICATION NO. 10/520,429
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANTS Eiichi TAKAHASHI et al.	
		FILING DATE July 13, 2005	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	1.	JP-A-2002-163034 w/ abst. & trans.	06/07/2002	JAPAN		
	2.	JP-A-09-321614 w/ abst. & trans.	12/12/1997	JAPAN		
	3.	JP-A-05-183337 w/ abst. & trans.	07/23/1993	JAPAN		
	4.	JP-U-03-098534	10/14/1991	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: October 6, 2005

APPENDIX

Statement of relevance for JP-U-03-98534 (10/14/1991)

The claim of the above application is as follows:

"A non-linear D/A converter characterized in that the converter comprising;

an R-2R ladder type resistor circuit having a number of steps equal to a number of bits of a digital signal input from outside,

an amplifier connected to an output terminal of the R-2R ladder type resistor circuit and outputs an analogue signal,

adding circuits each connected to each step of the R-2R ladder type resistor circuit,

a plurality of reference-voltage sources,

switches for connecting the plurality of reference-voltage sources and the adding circuits, and

a decoder for decoding the digital signal input from outside and controlling a connecting condition of the switches."